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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.		
10/786,962	02/25/2004	Scott Thomas Allen	5308-318	5308-318 9565		
20792 75	590 12/30/2005		EXAM	EXAMINER		
	EL SIBLEY & SAJOVE	RICHARDS, N DREW				
PO BOX 37428 RALEIGH, NO		ART UNIT	PAPER NUMBER			
			2815			
			DATE MAILED: 12/30/2009	DATE MAILED: 12/30/2005		

Please find below and/or attached an Office communication concerning this application or proceeding.

		Applic	ation No.	Applicant(s)				
		10/786	,962	ALLEN ET AL.				
Office Action Summary			ner	Art Unit				
		N. Drev	v Richards	2815				
Period fo	The MAILING DATE of this commun or Reply	ication appears on	the cover sheet with the	correspondence a	ddress			
WHIC - Exter after - If NC - Failu Any (	ORTENED STATUTORY PERIOD F CHEVER IS LONGER, FROM THE M nsions of time may be available under the provisions SIX (6) MONTHS from the mailing date of this come period for reply is specified above, the maximum st re to reply within the set or extended period for reply eply received by the Office later than three months and patent term adjustment. See 37 CFR 1.704(b).	AAILING DATE OF of 37 CFR 1.136(a). In no nunication. atutory period will apply and will, by statute, cause the	THIS COMMUNICATION event, however, may a reply be to will expire SIX (6) MONTHS from application to become ABANDON	ON. imely filed m the mailing date of this IED (35 U.S.C. § 133).				
Status								
1)⊠	Responsive to communication(s) file	ed on 26 Septembe	r 2005.					
2a) □		2b)⊠ This action is						
3) 🗌	Since this application is in condition for allowance except for formal matters, prosecution as to the merits is							
,	closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.							
Dispositi	on of Claims							
4)	. 4)⊠ Claim(s) <u>1-33</u> is/are pending in the application.							
•	4a) Of the above claim(s) <u>4-7 and 25-28</u> is/are withdrawn from consideration.							
5)	Claim(s) is/are allowed.							
6)🖂	Claim(s) <u>1-3,8,11-18,20-24,29,32 and 33</u> is/are rejected.							
7) 🖂	☑ Claim(s) <u>9,10,19,30 and 31</u> is/are objected to.							
8)								
Applicati	on Papers							
9)  🏹	The specification is objected to by th	e Examiner.						
10)⊠ The drawing(s) filed on <u>25 February 2004</u> is/are: a)□ accepted or b)⊠ objected to by the Examiner.								
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).								
	Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).							
11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.								
Priority ι	ınder 35 U.S.C. § 119							
12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  a) All b) Some * c) None of:  1. Certified copies of the priority documents have been received.  2. Certified copies of the priority documents have been received in Application No  3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  * See the attached detailed Office action for a list of the certified copies not received.								
2) 🔲 Notic 3) 🔯 Infori	t(s) e of References Cited (PTO-892) e of Draftsperson's Patent Drawing Review (f nation Disclosure Statement(s) (PTO-1449 or r No(s)/Mail Date <u>2/25/04,12/8/05</u> .		4) Interview Summa Paper No(s)/Mail 5) Notice of Informal 6) Other:	Date	rO-152)			

### **DETAILED ACTION**

#### Election/Restrictions

1. Applicant's election without traverse of Species II (claims 1-3, 8-24 and 29-33) in the reply filed on 9/26/05 is acknowledged.

#### Information Disclosure Statement

2. The listing of references in the specification is not a proper information disclosure statement. 37 CFR 1.98(b) requires a list of all patents, publications, or other information submitted for consideration by the Office, and MPEP § 609.04(a) states, "the list may not be incorporated into the specification but must be submitted in a separate paper." Therefore, unless the references have been cited by the examiner on form PTO-892, they have not been considered.

## **Drawings**

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the plurality or spacers having a checkerboard pattern, the thermal spacers aligned between adjacent unit cells, and the plurality of thermal spacers being non-uniform in size must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate

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prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

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4. The drawings are objected to because figure 4 contains an unlabeled featreu above layer 30. Since this feature is not labeled or discussed in the specification it is unclear as to what feature is depicted in the drawing. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief

description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

# Specification

5. The disclosure is objected to because of the following informalities: page 9 line 22 should recite "gate conductor 22" instead of "gate conductor 20" and the serial number needs to be supplied for the application mentioned on page 10 last line through page 11 line 3.

Appropriate correction is required.

#### Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
- 7. Claims 1-3, 8, 11-13, 16-18, 20, 21, 29, 32 and 33 are rejected under 35 U.S.C. 102(b) as being anticipated by Asano (EP 0725445 A1).

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Asano disclose in figure 6, for example, a high power high frequency semiconductor device comprising:

a plurality of unit cells connected in parallel, the unit cells each having a controlling electrode 2 and first 3 and second 4 controlled electrodes; and

a thermal spacer 5 dividing at least one of the unit cells into a first active portion and a second active portion spaced apart from the first portion by the thermal spacer, the controlling electrode and the first and second electrodes of the unit cell extending across the thermal spacer.

With regard to claim 2, Asano disclose in figure 6 the thermal spacer comprising a first and second thermal spacer that divides the unit cell into first, second and third portions with the electrodes extending over the thermal spacers as claimed.

With regard to claim 3, a third thermal spacer divides an adjacent unit cell into a first active portion and a second active portion with the electrodes extending over the thermal spacer as claimed.

With regard to claim 8, the thermal spacer includes an electrically inactive implanted region between the first and second active portions of the at least one unit cell.

With regard to claim 11, the thermal spacer is configured to provide a lower peak junction temperature than a corresponding unitary gate device for a particular set of operating conditions.

With regard to claim 12, the unit cells comprise a plurality of unit cells arranged in a linear array.

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With regard to claim 13, the controlling electrode is a gate finger and the first and second electrodes are source and drain electrodes.

With regard to claim 16, the thermal spacer is an electrically inactive region configured to not generate heat when in operation.

With regard to claim 17, Asano disclose:

a plurality of unit cells electrically connected in parallel each unit cell having a source region and a drain region (region under the source electrode 3 and drain electrode 4);

a plurality of gate electrodes 2 of the unit cells each connected in parallel;

a plurality of source electrodes 3 connected in parallel;

a plurality of drain electrodes 4 connected in parallel; and

a plurality of thermal spacers 5 that divide corresponding ones of the plurality of unit cells into at least a first active portion and a second active portion and wherein the gate electrodes, source electrodes, and drain electrodes cross over the thermal spacers.

With regard to claim 18, the unit cells comprise a plurality of unit cells arranged in a linear array.

With regard to claim 20, the plurality of thermal spacers are substantially uniform in size.

With regard to claim 21, as seen in figure 4a the thermal spacers 5 are formed to surround each unit cell such that the spacers are aligned between adjacent unit cells.

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With regard to claim 29, the thermal spacer includes an electrically inactive implanted region between the first and second active portions of the at least one unit cell.

With regard to claim 32, the thermal spacer is configured to provide a lower peak junction temperature than a corresponding unitary gate device for a particular set of operating conditions.

With regard to claim 33, the thermal spacer is an electrically inactive region configured to not generate heat when in operation.

# Claim Rejections - 35 USC § 103

- 8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
  - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 9. Claims 14, 15, 23 and 24 rejected under 35 U.S.C. 103(a) as being unpatentable over Asano (EP 0725445 A1) as applied to claims 1-3, 8, 11-13, 16-18, 20, 21, 29, 32 and 33 above, and further in view of D'Anna et al. (US Patent No. 6,521,923 B1).

Asano teach that their device is formed as an GaAs transistor. Asano do not teach the device being a silicon carbide MESFET or a GaN transistor.

D'Anna et al. teach that SiC (silicon carbide) and GaN materials are substitute materials for GaAs for microwave power devices. At the time of the invention it would have been obvious to one of ordinary skill in the art to use silicon carbide or GaN for the

transistor instead of GaAs. The reason for doing so is that D'Anna et al. teach that GaN and silicon carbide are well known substitute materials for GaAs to allow for microwave power FET devices.

10. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Asano (EP 0725445 A1) as applied to claims 1-3, 8, 11-13, 16-18, 20, 21, 29, 32 and 33 above, and further in view of Dupuy et al. (US Patent No. 6,140,184)

Asano do not teach the thermal spacers being non-uniform in size. Dupuy et al. teach across an array of cells the cells in the center are hotter than the cells in the edge. In view of this teaching of greater heat in the center, in combination with Asano's teaching of forming thermal spacer 5 to reduce channel temperature (or rather to reduce an increase in channel temperature during operation) it would have been obvious to form the thermal spacer 5 larger in the center of the array than along the edges of the array. It would have been obvious to form the thermal spacer in this non-uniform configuration so that the increased heat is adequately compensated for in the center while excess chip area is not consumed in the edges of the array.

# Allowable Subject Matter

11. Claims 9, 10, 19, 30 and 31 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

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12. The following is a statement of reasons for the indication of allowable subject matter: Prior art of record fails to teach disclose or suggest, either alone or in combination the features of claims 9, 10, 19, 30 and 31. Specifically, the prior art does not suggest forming the gate electrode having a greater cross sectional area or wider where it crosses the thermal spacer as recited in claims 9, 10, 30 and 31, nor does the prior art suggest forming the thermal spacers in a checkerboard pattern as recited in claim 19.

#### Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to N. Drew Richards whose telephone number is (571) 272-1736. The examiner can normally be reached on Monday-Friday 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

N. Drew Richards

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